REMARKS

Related to the Specification:

Applicant acknowledges the Examiner's suggestion related to the arrangement of the Specification and use of headings according to the guidelines of 37 C.F.R. 1.77(b). Submitted herewith is a Substitute Specification (not including claims or abstract), which is substantially identical to the original Specification except that section headings and paragraph reciting Applicant's claim of priority has been added.

No new matter has been thereby added to the Application.

Related to the Claims

Prior to this Amendment, Claims 1-6 were pending in the present application.

Claims 1-6 were amended.

Claims 7-20 were added.

Reconsideration of the claims is respectfully requested.

Claim Objections

Claims 2, 3, 5, and 6 were objected to because they began with an indefinite article. In response, Applicant has followed the Examiner's suggestion and replaced "A" or "An" at the beginning of each claim with -- The --.

Claim Rejections -- 35 U.S.C. § 102

Claims 1-4 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,933,771 to *Tiller et al.* (Claims 5 and 6 were actually rejected under 35 U.S.C. § 103, and their mention in paragraph 2 of the Office Action is assumed to be a typographical error.)

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Initially, Applicant respectfully points out that making this rejection, the Examiner cites (only) the circuit illustrated in FIG. 4 of the *Tiller* reference. There, addressing claim 1, the block numbered 30 is asserted to be a first stage differential amplifier (including transistors Q1 and Q2), transistors Q3 and Q4 a second stage, and transistors Q5 and Q6 a third stage, the second and third

stages each being coupled to one of two output branches of the first stage. Then, in reference to claim 2, it is asserted that the collectors of transistors Q3 and Q5 form the jointly-controlled sub-branches of the second output branch of the second differential amplifier. In FIG. 4 of *Tiller et al.*, however, the respective emitters of Q3 and Q5 are each coupled to different output branches of differential pair 30. This means that the transistors Q3 and Q5 of *Tiller et al.* cannot form the jointly-controlled sub-branches of the second output branch of the second differential amplifier. In fact, their collectors are purposely cross-connected in forming the quad mixer 34 (*Tiller et al.*, col. 4, lines 21-24). *Tiller et al.* therefore does not disclose or suggest the controllable amplifier circuit of claim 1 (or claim 2).

The claims have been amended to clarify relationship of the distinguishing features referred to above, and to make grammatical improvements.

Claims 3 and 4 depend from claim 1, and therefore are also distinguishable from *Tiller et al.* for the reasons provided above.

Therefore, the rejection of claims 1-4 under 35 U.S.C. § 102 has been overcome.

Claim Rejections -- 35 U.S.C. § 103

Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Tiller et al.* in view of U.S. Patent No. 5,945,847 to *Ransijn*. This rejection is respectfully traversed.

Initially claims 1 and 4, from which these claims depend, are distinguishable from the cited prior art for the reasons provided above.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or

suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

While Ransijn does discuss multi-stage amplifiers, it does not provide any teaching or suggestion to modify the disclosure of *Tiller et al.* to meet the claims of the present invention.

Therefore, the rejection of claims 5 and 6 under 35 U.S.C. § 103 has been overcome.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claims 1-6 were amended herein as follows:

1. (amended) A controllable amplifier arrangement comprising:

a first differential amplifier stage having a first and a second output branch[,] ;

a second differential amplifier stage [which] that is coupled to the first output branch of the first differential amplifier stage [and has], the second differential amplifier stage having [at least] a first output branch and at least a second output branch [, at which] for controllably dividing a first current in the first output branch of the first differential amplifier stage [is controllably divided] into partial currents[,] ;

a third differential amplifier stage [which] that is coupled to the second output branch of the first differential amplifier stage [and has], the third differential amplifier stage having [at least] a first output branch and at least a second output branch [, at which] for controllably dividing a second current in the second output branch of the first differential amplifier stage [is controllably divided] into partial currents[,] ;

a first load impedance coupled to one of the [first] output branches of the second differential amplifier stage for generating a first output voltage from the partial current flowing in said one of the first output branches of the second differential amplifier stage[,] ; and

a second load impedance coupled to one of the [first] output branches of the third differential amplifier stage for generating a second output voltage from the partial current flowing in said one of the first output branches of the third differential amplifier stage[,] ;

wherein the first and the second load impedance are bridged to a predetermined part by at least one of the second output branches of the second and third differential amplifier stages, respectively.

2. (amended) [A] The controllable amplifier arrangement as claimed in claim 1, [characterized in that] wherein said one of the second output branches of the second differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the first load impedance, and in that said one of the second output branches of the third differential amplifier stage has two jointly controlled sub-branches, a first sub-branch of which is coupled to the second load impedance.

3. (amended) [A] The controllable amplifier arrangement as claimed in claim 1, [characterized in that] wherein said one of the second output branches of the second differential amplifier stage is coupled to a tap on the first load impedance, and said one of the second output branches of the third differential amplifier stage is coupled to a tap on the second load impedance.

4. (twice amended) An arrangement for processing electric signals, [characterized by] comprising at least one controllable amplifier arrangement [as claimed in claim 1], the controllable amplifier comprising:

a first differential amplifier stage having a first and a second output branch;

a second differential amplifier stage that is coupled to the first output branch of the first differential amplifier stage , the second differential amplifier stage having a first output branch and at least a second output branch for controllably dividing a first current in the first output branch of the first differential amplifier stage into partial currents;

a third differential amplifier stage that is coupled to the second output branch of the first differential amplifier stage, the third differential amplifier stage having a first output branch and at least a second output branch for controllably dividing a second current in the second output branch of the first differential amplifier stage into partial currents;

a first load impedance coupled to one of the output branches of the second differential amplifier stage for generating a first output voltage from the partial current flowing in said one of the first output branches of the second differential amplifier stage; and

a second load impedance coupled to one of the output branches of the third differential amplifier stage for generating a second output voltage from the partial current flowing in said one of the first output branches of the third differential amplifier stage.

5. (amended) [An] The arrangement for processing electric signals as claimed in claim 4, comprising at least two controllable amplifier arrangements [as claimed in any one of claims 1 to 3], [characterized in that] wherein the second and the third differential amplifier stage of the controllable amplifier arrangements are controllable by means of common control signals and have control characteristics which are mutually offset in such a way that the partial currents flowing in the output branches of the second and the third differential amplifier stage are reversed in the individual controllable amplifier arrangements at different values of the common control signals.

6. (amended) [An] The arrangement for processing electric signals as claimed in claim 5, [characterized in that] wherein the output branches of the second and the third differential amplifier stage are formed with transistors whose main current paths have current conveying cross-sectional areas whose dimensioning determines the reversal of the partial currents in the output branches of the second and third differential amplifier stages of the individual controllable amplifier arrangements at the different values of the common control signals in the individual controllable amplifier arrangements.

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: Dec. 20, 2002

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